IFW

Patent

Docket No.: LOVO-051.CON

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.					
Date of Deposit:	09/15/04	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): William Planey

Application No.: 10/728,449 Group Art Unit:

Filed: 12/05/03 Examiner:

Title: FLIP-CHIP PACKAGING

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..X.. Information Disclosure statement (2 sheets)
..... Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: REFERENCES

Fee Calculation (for other than a small entity)					
Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$0.00
Other:					$0.00
Total Fees					$0.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 45547

Respectfully submitted,

Date: 9/15/2004

By: _____
Anthony C. Murabito
Reg. No. 35,295

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: LOVO-051.CON

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Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date

The Examiner's attention is respectfully directed to the following related documents:

H. Ogiwara, M. Hayakawa, T. Nishimura and M. Nakaoka; "HIGH-FREQUENCY INDUCTION HEATING INVERTER WITH MULTI-RESONANT MODE USING NEWLY DEVELOPED NORMALLY-OFF TYPE STATIC INDUCTION TRANSISTORS"; Department of Electrical Engineering, Ashikaga Institute of Technology, Japan; Department of Electrical Engineering, Oita University, Japan; Department of Electrical Engineering, Kobe University, Japan; pages 1017-1023

J. Baliga; "HIGHVOLTAGE JUNCTION-GATE FIELD EFFECT TRANSISTOR WTH RECESSED GATES"; IEEE Transactions on Electron Devices; Vol. ED-29; No. 10; Oct. 1982

J. M. C. Stork et al.; "SMALL GEOMETRY DEPLETED BASE BIPOLAR TRANSISTORS (BSIT)- VLSI DEVICES?"; IEEE Transactions on Electron Devices; Vol. ED-28; No. 11; Nov. 1981

Nishizawa et al.; "ANALYSIS OF STATIC CHARACTERISTICS OF A BIPOLAR MODE SIT (BSIT)"; IEEE Transactions on Electron Devices; Vol. ED-29; No. 11; Aug. 1982

Caruso et al.; "PERFORMANCE ANALYSIS OF A BIPOLAR MODE FET (BMFET) WITH NORMALLY OFF CHARACTERISTICS"; IEEE Transactions on Power Electronics; Vol. 3; No. 2; April 1988

Nishizawa et al.; "FIELDEFFECT TRANSISTOR VERSUS ANALOG TRANSISTOR (STATIC INDUCTION TRANSISTOR)"; IEEE Transactions on Electron Devices; Vol. ED-24; No. 4; April 1975

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): William Planey

Application No.: 10/728,449 Group Art Unit:

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Title: FLIP-CHIP PACKAGING

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	B							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C	H. Ogiwara, M. Hayakawa, T. Nishimura and M. Nakaoka; "HIGH-FREQUENCY INDUCTION HEATING INVERTER WITH MULTI-RESONANT MODE USING NEWLY DEVELOPED NORMALLY-OFF TYPE STATIC INDUCTION TRANSISTORS"; Department of Electrical Engineering, Ashikaga Institute of Technology, Japan; Department of Electrical Engineering, Oita University, Japan; Department of Electrical Engineering, Kobe University, Japan; pages 1017-1023
	D	J. Baliga; "HIGHVOLTAGE JUNCTION-GATE FIELD EFFECT TRANSISTOR WTH RECESSED GATES"; IEEE Transactions on Electron Devices; Vol. ED-29; No. 10; Oct. 1982
	E	J. M. C. Stork et al.; "SMALL GEOMETRY DEPLETED BASE BIPOLAR TRANSISTORS (BSIT)- VLSI DEVICES?"; IEEE Transactions on Electron Devices; Vol. ED-28; No. 11; Nov. 1981
	F	Nishizawa et al.; "ANALYSIS OF STATIC CHARACTERISTICS OF A BIPOLAR MODE SIT (BSIT)"; IEEE Transactions on Electron Devices; Vol. ED-29; No. 11; Aug. 1982
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Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.